UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,495	02/20/2004	Yung-Cheng Chen	N1085-00251 [TSMC2003-083	2148

54657 7590 05/17/2010
DUANE MORRIS LLP (TSMC)
IP DEPARTMENT
30 SOUTH 17TH STREET
PHILADELPHIA, PA 19103-4196

EXAMINER	
NORTON, JENNIFER L	

ART UNIT	PAPER NUMBER
2121	

MAIL DATE	DELIVERY MODE
05/17/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,495	CHEN ET AL.	
	Examiner	Art Unit	
	JENNIFER L. NORTON	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. The following is a **Non-Final Office Action** in response to the After-Final Amendment/Remarks received on 23 April 2010. Claim 2 was previously cancelled. Claims 1 and 3-22 are pending in this application.

Response to Arguments

2. Applicant's arguments, see Remarks pgs. 6-13 filed 23 April 2010 with respect to claims 1 and 3-22 under 35 U.S.C. 103(a) have been considered but are moot in view of the new ground(s) of rejection.

3. With respect to the Applicant's arguments, "Park teaches away from changing exposure energy as his entire disclosure is directed to precluding the need to alter or control exposure energy." The Examiner respectfully disagrees. See MPEP 2123, recited below for convenience:

> MPEP 2123 states:
>
> "Disclosed examples and preferred embodiments do not constitute a teaching away from a broader disclosure or nonpreferred embodiments. In re Susi, 440 F.2d 442, 169 USPQ423 (CCPA 1971). "A known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use." In re Gurley, 27 F.3d 551, 554, 31 USPQ2d 1130, 1132 (Fed. Cir. 1994) (The invention was directed to an epoxy impregnated fiber-reinforced printed circuit material. The applied prior art reference taught a printed circuit material similar to that of the claims but impregnated with polyesterimide resin instead of epoxy. The reference, however, disclosed that epoxy was known for this use, but that epoxy impregnated circuit boards have "relatively acceptable dimensional

stability" and "some degree of flexibility," but are inferior to circuit boards impregnated with polyesterimide resins. The court upheld the rejection concluding that applicant's argument that the reference teaches away from using epoxy was insufficient to overcome the rejection since "Gurley asserted no discovery beyond what was known in the art." 27 F.3d at 554, 31 USPQ2d at 1132.). Furthermore, "[t]he prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed...." In re Fulton,391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004).

Furthermore, Park teaches

"Another object is to provide a system for adjusting a photo-exposure time capable of enhancing a uniformity of a photoresist pattern by reflecting a feedback of factors to be compensated obtained from a post-exposure evaluation of the photo-exposure result and a feed forward of factors to be cured, obtained before a photo-exposure process." (col. 2, lines 50-55)

"During processing, a wafer is first provided to a pre-exposure step process. In the pre-exposure step process 10, a silicon-nitride film is preferably deposited uniformly on the surface of a wafer. Next, the wafer is provided to a photo-exposure process 20. In the photo-exposure process 20, a photoresist is formed over a whole surface of the wafer, and then baking, exposing, and developing are sequentially performed. After the development portion of the photo-exposure process, the wafer then progresses to the after-development inspection (ADI) process 30, which inspects and measures a line width of the photoresist pattern formed after the photo-exposure process 20. The wafer is then transferred to the next process using a photoresist mask such as an etching or an ion implantation process. (col. 4, lines 59-67 and col. 5, lines 1-3)

"In the photo-exposure process 20, information regarding the photo-exposure time is provided to the photo-exposure unit 50 together with other conditioning parameters, such as characteristics of the photoresist material and light source, baking temperature and time, development conditions, and so on. It is desirable that a photo-exposure time be classified and managed with the unique number of reticles because photo-exposure time may vary by reticles even in the same step and equipment." (col. 5, lines 20-28)

> "an inspection unit for generating an inspection value by measuring an aspect of the semiconductor device after it has been subjected to the photo-exposure step, and providing the inspection value as feed back data;" (col. 8, lines 56-59)

In summary, Park teches to a feedback process that adjusts (i.e. compensates) a plurality of factors, as well as, providing the photo-exposure process with information regarding exposure time together with other conditioning parameters, such as characteristics of the photoresist material and light source, baking temperature and time, development conditions, and so on. Hence, Park teaches to adjusting a plurality of parameters in a semiconductor process, and providing a photo-exposure process with a variety of conditioning parameters.

4. Claims 1 and 3-22 stand rejected under 35 U.S.C. 103(a) as set forth below.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3, 4 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,825,912 B2 (hereinafter Park) in view of U.S. Patent No. 6,630,362 B1 (hereinafter Lensing).

7. As per claim 1, Park teaches a method for controlling exposure on a patterned wafer substrate, comprising the steps of:

controlling the exposure (col. 2, lines 50-55, col. 3, lines 26-28 and col. 8, lines 43-46) with a feedback process control signal (col. 3, lines 40-51, col. 4, lines 66-67, col. 5, lines 1-3, col. 8, lines 56-59 and Fig. 1, element 30) of critical dimension (col. 5, lines 35-50; i.e. line width),

and further controlling the exposure (col. 2, lines 50-55, col. 3, lines 26-28 and col. 8, lines 43-46) with a feed forward process control signal (col. 3, lines 21-25 and 29-39, col. 5, lines 13-18 and col. 8, lines 47-55 and Fig. 1, element 10) of a compensation amount that compensates for thickness variations (col. 7, lines 35-45, 53-56 and 62-67, col. 8, lines 1-11 and Fig. 1, element 40) in a subjacent layer beneath a top layer (col. 3, lines 21-24, col. 4, lines 59-62 and col. 5, lines 13-18; i.e. a silicon-nitride film formed in the pre-exposure process), by combining the feed forward process control signal with the feedback process control signal (col. 3, lines 18-20 and 51-59 and col. 8, lines 60-63) to control the exposure (col. 3, lines 60-65 and col. 8, lines 43-46) used in patterning the top layer (col. 3, lines 21-24, col. 4, lines 63-66 and col. 5, lines 13-27; i.e. a photoresist formed in the photo-exposure process), the critical dimension being one of a width, a spacing and an opening of the patterned wafer substrate (col. 5, lines 40-43).

Park does not expressly teach to exposure energy (per definition of exposure energy on pg. 1, par. [0002] of Applicant's Specification), and the top layer being a non-photoresist layer.

Lensing teaches to controlling the exposure energy in semiconductor manufacturing (col. 6, lines 56-67; i.e. controlling the exposure energy of the stepper).

Lensing does not expressly teach within the same embodiment a top layer being a non-photoresist layer.

Lensing teaches a top layer being a non-photoresist layer (col. 7, lines 39-44 and 53-59; i.e. a nitride layer and a oxide layer).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Park to include controlling the exposure energy in semiconductor manufacturing; and to include within the same embodiment a top layer being a non-photoresist layer to detect variations and adjust parameters of equipment in the manufacture of semiconductors to correct nonconformity (Lensing: col. 7, lines 23-32).

8. As per claim 3, Park teaches as set forth above supplying the feed forward process control signal by a feed forward controller (col. 5, lines 13-18 and Fig. 1, element 40).

9. As per claim 4, Park teaches as set forth above the subjacent layer comprises an interlayer (col. 3, lines 21-24 and col. 5, lines 13-18; i.e. a silicon-nitride film of a reflection barrier layer).

10. As per claim 9, Park teaches as set forth above calculating the compensation amount according to a polynomial function with higher order coefficients set at zero (col. 7, lines 35-45, 53-56 and 62-67 and col. 8, lines 1-11).

11. As per claim 10, Park teaches as set forth above calculating the compensation amount according to a linear function (col. 7, lines 35-45, 53-56 and 62-67 and col. 8, lines 1-11).

12. As per claim 11, Park teaches as set forth above further comprising the steps calculating the compensation amount according to a segmented linear function (col. 7, lines 35-45, 53-56 and 62-67 and col. 8, lines 1-11).

13. Claims 5-8 and 12-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park in view of Lensing in further view of U.S. Patent No. 6,798,529 (hereinafter Saka).

14. As per claim 5, Park teaches controlling the exposure energy (col. 2, lines 50-55, col. 3, lines 26-28 and col. 8, lines 43-46) by a feed forward process control signal

utilizes a signal measurement of thickness (col. 3, lines 21-24 and col. 5, lines 13-27; i.e. a silicon-nitride film of a reflection barrier layer).

Park does not expressly teach a measurement of thickness remaining of the interlayer after chemical mechanical planarization thereof.

Lensing does not expressly teach a measurement of thickness remaining of the interlayer after chemical mechanical planarization thereof.

Saka teaches to a measurement of thickness remaining of the interlayer after chemical mechanical planarization thereof (col. 8, lines 61-63 and col. 13, lines 27-33).

Therefore, it would have been obvious to a person of ordinary skill in n the art at the time of Applicant's invention to modify the teaching of Park in view of Lensing to include a measurement of thickness remaining of the interlayer after chemical mechanical planarization thereof to continuously and in-situ, monitor localized regions of a wafer surface during the chemical mechanical planarization process (col. 5, lines 38-40).

15. As per claim 6, Park teaches calculating the compensation amount according to a polynomial function with a coefficient of the function (col. 7, lines 35-45, 53-56 and 62-67, col. 8, lines 1-11) being based on a measurement of a thickness (col. 5, lines 13-18, col. 7, lines 20-27 and col. 10, lines 5-9).

Park does not expressly teach a measurement of a remaining thickness of a planarized interlayer.

Lensing does not expressly a measurement of a remaining thickness of a planarized interlayer.

Saka teaches to a measurement of a remaining thickness of a planarized interlayer (col. 8, lines 61-63 and col. 13, lines 27-33).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicant's invention to modify the teaching of Park in view of Lensing to include a measurement of a remaining thickness of a planarized interlayer to continuously and in-situ, monitor localized regions of a wafer surface during the chemical mechanical planarization process (col. 5, lines 38-40).

16. As per claim 7, Park teaches to calculating the feedback process control signal of critical dimension measurement of a layer (col. 5, lines 35-50; i.e. line width).

Park does not expressly teach calculating the feedback process control signal of critical dimension measurement of a top layer in a previous manufacturing lot.

Lensing does not expressly teach calculating the feedback process control signal of critical dimension measurement of a top layer in a previous manufacturing lot.

Saka teaches to calculating the feedback process control signal of critical dimension measurement of a top layer in a previous manufacturing lot (col. 12, lines 32-35; i.e. run-to-run).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicant's invention to modify the teaching of Park in view of Lensing to include calculating the feedback process control signal of critical dimension measurement of a top layer in a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the chemical mechanical planarization process (col. 5, lines 38-40).

17. As per claim 8, Park teaches calculating the compensation amount according to a polynomial function with a coefficient of the function (col. 7, lines 35-45, 53-56 and 62-67, col. 8, lines 1-11) being based on a measurement of a thickness of the subjacent layer (col. 3, lines 21-24 and col. 5, lines 13-18; i.e. a silicon-nitride film of a reflection barrier layer); and calculating the feedback process control signal of critical dimension measurement (col. 5, lines 35-50; i.e. line width).

Park does not expressly teach a measurement of a remaining thickness of the subjacent layer, the subjacent layer being a planarized layer and to calculating the feedback process control signal of critical dimension measurement of a top layer in a previous manufacturing lot.

Lensing does not expressly teach a measurement of a remaining thickness of the subjacent layer, the subjacent layer being a planarized layer and to calculating the feedback process control signal of critical dimension measurement of a top layer in a previous manufacturing lot.

Saka teaches to a measurement of a remaining thickness of the subjacent layer (col. 8, lines 61-63 and col. 13, lines 27-33), the subjacent layer being a planarized layer (col. 8, lines 61-63 and col. 13, lines 27-33) and to calculating the feedback process control signal of critical dimension measurement of a top layer in a previous manufacturing lot (col. 12, lines 32-35; i.e. run-to-run).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicant's invention to modify the teaching of Park in view of Lensing to include a measurement of a remaining thickness of the subjacent layer, the subjacent layer being a planarized layer and to calculating the feedback process control signal of critical dimension measurement of a top layer in a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the chemical mechanical planarization process (col. 5, lines 38-40).

18. As per claim 12, Park teaches a system for controlling exposure on a first patterned wafer substrate, comprising:

a feed forward controller (Fig. 1, element 40) providing a feed forward control signal (col. 5, lines 13-18) to an exposure apparatus (col. 8, lines 27-30 and Fig. 1, element 50) based on a thickness measurement of an interlayer of the first patterned wafer substrate for controlling the exposure focused on a top layer of the first patterned wafer substrate (col. 2, lines 50-55, col. 3, lines 26-28 and col. 8, lines 43-46), and

a feedback controller (col. 5, lines 38-39 and Fig. 1, element 60) providing a feedback exposure control signal (col. 5, lines 35-38 and Fig. 1, element 30) to the exposure apparatus (col. 8, lines 27-30 and Fig. 1, element 50) based on critical dimension measurement of a top layer of a patterned wafer substrate (col. 5, lines 35-50), the critical dimension being one of a width, a spacing and an opening of the patterned wafer substrate (col. 5, lines 40-43) wherein a combiner (col. 3, lines 18-21, col. 8, lines 27-30 and 60-63 and Fig. 1, element 70) combines the feed forward control signal and the feedback exposure control signal to produce a combined signal that is provided to the exposure apparatus (col. 3, lines 25-27 and 60-65 and col. 8, lines 27-30 and 43-46).

Park does not expressly teach exposure energy (per definition of exposure energy on pg. 1, par. [0002] of Applicant's Specification), a critical dimension measurement of a top layer of a second patterned wafer substrate of a previous manufacturing lot, and the top layer being a non-photoresist layer.

Lensing teaches to controlling the exposure energy in semiconductor manufacturing (col. 6, lines 56-67; i.e. controlling the exposure energy of the stepper).

Lensing does not expressly teach within the same embodiment a top layer being a non-photoresist layer a top layer being a non-photoresist layer and does not expressly teach a critical dimension measurement of a top layer of a second patterned wafer substrate of a previous manufacturing lot.

Lensing teaches a top layer being a non-photoresist layer (col. 7, lines 39-44 and 53-59; i.e. a nitride layer and a oxide layer).

Saka teaches to a critical dimension measurement of a top layer of a second wafer substrate (col. 12, lines 25-28 and col. 33, lines 4-5) of a previous manufacturing lot (col. 6, lines 58-60, col. 9, lines 28-33 and col. 12, lines 32-35; i.e. run-to-run).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicant's invention to modify the teaching of Park to include controlling the exposure energy in semiconductor manufacturing, and to include within the same embodiment a top layer being a non-photoresist layer to detect variations and adjust parameters of equipment in the manufacture of semiconductors to correct nonconformity (Lensing: col. 7, lines 23-32); and a critical dimension measurement of a top layer of a second patterned wafer substrate of a previous manufacturing lot to

continuously and in-situ, monitor localized regions of a wafer surface during the chemical mechanical planarization process (Saka: col. 5, lines 38-40).

19. As per claim 13, Park teaches as set forth above a thickness measurement device (col. 5, lines 13-16 and Fig. 1, element 10) providing thickness measurement data to the feed forward controller (col. 5, lines 16-18 and Fig. 1, element 40).

20. As per claim 14, Park teaches as set forth above a critical dimension measurement device (col. 5, lines 35-38 and Fig. 1, element 30) providing critical dimension measurement data to the feedback controller (col. 5, lines 38-39 and Fig. 1, element 60).

21. As per claim 15, Park teaches as set forth above thickness measurement device (col. 5, lines 13-16 and Fig. 1, element 10) providing thickness measurement data to the feed forward controller (col. 5, lines 16-18 and Fig. 1, element 40) and a critical dimension measurement device (col. 5, lines 35-38 and Fig. 1, element 30) providing critical dimension measurement data to the feedback controller (col. 5, lines 38-39 and Fig. 1, element 60).

22. As per claim 16, Park teaches a thickness measurement device (col. 5, lines 13-16 and Fig. 1, element 10) providing thickness measurement data of layer (col. 3, lines

21-24 and col. 5, lines 13-18; i.e. a silicon-nitride film of a reflection barrier layer) of the first patterned wafer substrate to the feed forward controller (col. 5, lines 16-18 and Fig. 1, element 40).

Park does not expressly teach a thickness measurement device providing thickness measurement data of a shallow trench isolation layer of the first patterned wafer substrate to the feed forward controller.

Lensing teaches a thickness measurement device (col. 6, lines 22-37 and Fig. 6, element 540) providing thickness measurement of a patterned wafer substrate (col. 7, lines 23-27).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Park to include a thickness measurement device providing thickness measurement of a patterned wafer substrate to detect variations and adjust parameters of equipment in the manufacture of semiconductors to correct nonconformity (col. 7, lines 23-32).

23. As per claim 17, Park teaches a critical dimension measurement device (Fig. 1, element 30) providing critical dimension measurement data (i.e. line width) of a poly-gate of wafer substrate (col. 5, lines 35-50).

Park does not expressly teach a critical dimension measurement device providing critical dimension measurement data of a poly-gate of wafer substrate of a previous manufacturing lot.

Lensing does not expressly teach a critical dimension measurement device providing critical dimension measurement data of a poly-gate of wafer substrate of a previous manufacturing lot.

Saka teaches a critical dimension measurement device providing critical dimension measurement data of a poly-gate of wafer substrate (col. 12, lines 25-28 and col. 33, lines 4-5) of a previous manufacturing lot (col. 6, lines 58-60, col. 9, lines 28-33 and col. 12, lines 32-35; i.e. run-to-run).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Park in view of Lensing to include a critical dimension measurement device providing critical dimension measurement data of a poly-gate of wafer substrate of a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the chemical mechanical planarization process (col. 5, lines 38-40).

24. As per claim 18, Park teaches a thickness measurement device (col. 5, lines 13-16 and Fig. 1, element 10) providing thickness measurement data of layer (col. 3, lines 21-24 and col. 5, lines 13-18; i.e. a silicon-nitride film of a reflection barrier layer) of the

first patterned wafer substrate to the feed forward controller (col. 5, lines 16-18 and Fig. 1, element 40), and

a critical dimension measurement device (Fig. 1, element 30) providing critical dimension measurement data (i.e. line width) of a poly-gate (col. 5, lines 35-50).

Park does not expressly teach a thickness measurement device providing thickness measurement data of a shallow trench isolation layer of the first patterned wafer substrate to the feed forward controller and a critical dimension measurement device providing critical dimension measurement data of a poly-gate of a previous manufacturing lot.

Lensing teaches a thickness measurement device (col. 6, lines 22-37 and Fig. 6, element 540) providing thickness measurement of a patterned wafer substrate (col. 7, lines 23-27).

Lensing does not expressly teach a critical dimension measurement device providing critical dimension measurement data of a poly-gate of a previous manufacturing lot.

Saka teaches a critical dimension measurement device providing critical dimension measurement data of a poly-gate of wafer substrate (col. 12, lines 25-28 and col. 33, lines 4-5) of a previous manufacturing lot (col. 6, lines 58-60, col. 9, lines 28-33 and col. 12, lines 32-35; i.e. run-to-run).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Park to include a thickness measurement device providing thickness measurement of a patterned wafer substrate to detect variations and adjust parameters of equipment in the manufacture of semiconductors to correct nonconformity (Lensing: col. 7, lines 23-32); and a critical dimension measurement device providing critical dimension measurement data of a poly-gate of wafer substrate of a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the chemical mechanical planarization process (Saka: col. 5, lines 38-40).

25. As per claim 19, Park teaches as set forth above the feed forward controller is user configurable by having one or more polynomial coefficients set to zero in a polynomial function model (col. 7, lines 35-45, 53-56 and 62-67 and col. 8, lines 1-11).

26. As per claim 20, Park teaches as set forth above the feed forward controller is user configurable by having one or more polynomial coefficients set to zero in a polynomial function model (col. 7, lines 35-45, 53-56 and 62-67 and col. 8, lines 1-11).

27. As per claim 21, Park teaches a thickness measurement device (col. 5, lines 13-16 and Fig. 1, element 10) providing thickness measurement data of layer (col. 3, lines 21-24 and col. 5, lines 13-18; i.e. a silicon-nitride film of a reflection barrier layer) of the

first patterned wafer substrate to the feed forward controller (col. 5, lines 16-18 and Fig. 1, element 40).

Park does not expressly teach a thickness measurement device providing thickness measurement data of a shallow trench isolation layer of the first patterned wafer substrate to the feed forward controller.

Lensing teaches a thickness measurement device (col. 6, lines 22-37 and Fig. 6, element 540) providing thickness measurement of a patterned wafer substrate (col. 7, lines 23-27).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Park to include a thickness measurement device providing thickness measurement of a patterned wafer substrate to detect variations and adjust parameters of equipment in the manufacture of semiconductors to correct nonconformity (col. 7, lines 23-32).

28. As per claim 22, Park teaches a critical dimension measurement device (Fig. 1, element 30) providing critical dimension measurement data (i.e. line width) of a poly-gate of a wafer substrate (col. 5, lines 35-50).

Park does not expressly teach a critical dimension measurement device providing critical dimension measurement data of a poly-gate of the second patterned wafer substrates of a previous manufacturing lot.

Lensing does expressly teach a critical dimension measurement device providing critical dimension measurement data of a poly-gate of the second patterned wafer substrates of a previous manufacturing lot.

Saka teaches a critical dimension measurement device providing critical dimension measurement data of a poly-gate of the second patterned wafer substrates (col. 12, lines 25-28 and col. 33, lines 4-5) of a previous manufacturing lot (col. 6, lines 58-60, col. 9, lines 28-33 and col. 12, lines 32-35; i.e. run-to-run).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Park in view of Lensing to include a critical dimension measurement device providing critical dimension measurement data of a poly-gate of the second patterned wafer substrates of a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the chemical mechanical planarization process (col. 5, lines 38-40).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JENNIFER L. NORTON whose telephone number is (571)272-3694. The examiner can normally be reached on Monday-Friday between 9:00 a.m. - 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Albert DeCady/
Supervisory Patent Examiner
Art Unit 2121

/JLN/